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In re PATENT application of:)
Shunpei YAMAZAKI et al.)
Serial No. 08/504,225) Art Unit: 1107
Filed: July 19, 1995) Examiner: M. Wilczewski
For: SEMICONDUCTOR DEVICE AND)
METHOD FOR FORMING THE SAME)

VERIFICATION OF TRANSLATION

Honorable commissioner of patents and Trademarks
Washington, D.C. 20231

Sir:

I, Ikuko Noda, 3-G, 1551, Hase, Atsugi-shi, Kanagawa-ken 243 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the Japanese Patent Application No. 3-65418 filed on March 6, 1991; and

that to the best of my knowledge and belief the following is a true and correct translation of the Japanese Patent Application No. 3-65418 filed on March 6, 1991.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 24th day of April , 1997

Ikuko Noda

Name: Ikuko Noda

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[Title of the Invention] An insulating gate type field effect semiconductor device and a manufacturing method thereof

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[Inventor]
[Address] 398 Hase, Atsugi-shi, Kanagawa-ken
c/o Semiconductor Energy Laboratory Co., Ltd.
[Name] Shunpei Yamazaki
[Inventor]
[Address] 398 Hase, Atsugi-shi, Kanagawa-ken
c/o Semiconductor Energy Laboratory Co., Ltd.
[Name] Akira Mase

[Applicant]
[Identification Number] 000153878
[Zip Code] 243
[Address] 398 Hase, Atsugi-shi, Kanagawa-ken
[Name] Semiconductor Energy Laboratory Co., Ltd.
[Representative] Shunpei Yamazaki

[List of Attachment]
[Attachment] Specification 1
[Attachment] Drawing 1
[Attachment] Abstract 1

[NAME OF DOCUMENT] Specification

[TITLE OF THE INVENTION]

An insulating gate type field effect semiconductor device and a manufacturing method thereof

[WHAT IS CLAIMED IS]

[Claim 1] An insulating gate type field effect semiconductor device, said insulating gate type field effect semiconductor device in a thin film structure provided on a substrate, wherein aluminum is utilized for gate electrode and at least side surface of said gate electrode is covered with aluminum oxide.

[Claim 2] An insulating gate type field effect semiconductor device, said insulating gate type field effect semiconductor device in a thin film structure provided on a substrate, wherein gate electrode is aluminum and at least side surface of said gate electrode is covered with aluminum oxide, and contact holes for output electrodes of source or drain region approximately in the same position as the end face of oxide of said aluminum are provided.

[Claim 3] A method of manufacturing an insulating gate field effect semiconductor device comprising the processes of: forming a semiconductor film mainly comprising silicon including hydrogen on a substrate; heating said semiconductor film mainly comprising silicon to change its character to a structure having crystal character; forming a gate electrode from aluminum; oxidizing peripheral portion of said gate electrode to form aluminum oxide at least on a side face.

[Claim 4] A method of manufacturing an insulating gate field effect semiconductor device comprising the processes of: forming a semiconductor film mainly comprising silicon including hydrogen on a substrate; heating said semiconductor film mainly comprising silicon to change its character to a structure having crystal character; forming a gate electrode from aluminum; oxidizing peripheral portion of said gate electrode to form aluminum oxide at least on a side face; and forming contact holes for output electrodes of source or drain region approximately in the same position as the end face of said gate electrode and aluminum oxide.

[Detailed Description of the Invention]

[0001]

[Field for Industrial Use]

The present invention relates to a thin film transistor, and is especially applicable to a liquid crystal display device and an image sensor device of perfect adhesive type.

[0002]

[Prior Art]

The insulating gate type field effect semiconductor device conventionally known is widely utilized for many categories. This semiconductor device is formed on a silicon substrate, and utilized as an IC or LSI by mechanically integrating many semiconductor devices.

[0003]

On the other hand, thin film type insulating gate type field effect semiconductor device (hereinafter called as TFTs) formed by depositing a thin film not only on a silicon substrate but on an insulating substrate and the like is getting utilized attentively for a switching device portion and a portion of a driving circuit of a picture element of a liquid crystal display device, and a read circuit element of an adhesive image sensor.

[0004]

Because the TFTs are formed by depositing thin films on an insulating substrate by a gas phase method as above mentioned, it can be formed under a low formation atmosphere temperature up to 500℃. Inexpensive soda glass and boro-silicate glass can be utilized as a substrate.

[0005]

In this way, the TFTs can be formed on an inexpensive substrate, and the maximum size of it is only limited to the size of an apparatus which forms a thin film by a gas phase method, and transistors can be formed easily on a large-area substrate. Therefore, use for a liquid crystal display in a matrix structure with many picture elements and for one-dimensional or two-dimensional image sensor is expected, and partly is made real.

[0006]

A typical structure of the TFTs is schematically shown in Fig. 2.

[0007]

In Fig. 2, reference numeral 1 is an insulating substrate comprising glass, 2 is a thin film semiconductor comprising an amorphous semiconductor, 3 is a source, drain region, 7 is a source, drain electrode, and 11 is a gate electrode.

[0008]

As above mentioned, because the semiconductor layer utilized for such TFTs as this is formed by a gas phase method, mobility of holes and electrodes was much less than that of a semiconductor layer utilized for conventional IC and LSI. Usually it is heated to crystallize the semiconductor layer 2.

[0009]

[Problems the invention intends to solve]

As the prior art shown in Fig. 2, usually a gate electrode 11 is covered with an interlayer insulator 4 of a comparatively thick silicon nitride film,silicon oxide film and the like. A contact hole is provided to this interlayer insulator by photolithography method, electrically contacting the source, drain electrode 7 with the source, drain region 3. If a feeding point to a source or drain is provided to this position, distance L from each feeding point to the end portion of the channel gets pretty longer.

[0010]

As above mentioned, because mobility of carriers is low by nature in the TFTs formed by a thin film low temperature process, conductivity is low even after impurity doping. Therefore, resistance is produced in the part of distance L. This caused decrease of frequency character of the TFTs and increase of ON resistance.

[0011]

If this distance L gets longer, naturally an area for a set of TFTs increased. It was difficult to provide TFTs by the decided number on a substrate of limited size.

[0012]

Therefore, in the present invention, TFTs were improved to shorten the distance L from a feeding point to a source or drain region adjacent to a channel region of an insulating gate type field effect semiconductor to the channel end portion.

[0013]

[Means to solve the problems]

The TFTs of the present invention is characterized by utilizing aluminum as a gate electrode, and at least a side face of said gate electrode is covered with oxide of aluminum. It is also characterized in that a contact hole for an output electrode of source or drain region is provided approximately in the same position of the end face of oxide of

aluminum on the side face of this gate electrode.

[0014]

Moreover, to increase mobility of carriers in a semiconductor layer, the value of this mobility is improved by changing the layer to a structure with crystal character by heating a semiconductor film mainly comprising said silicon after its formation. Moreover, to make the distance L from the feeding point the least, the gate electrode is formed of aluminum, and aluminum oxide is formed on at least the side face by oxidizing the peripherals of this gate electrode.

[0015]

Moreover, with the use of an aluminum oxide film existing in this gate electrode and its peripheral portion, a contact hole for an output electrode of the source or drain portion is formed in self-align method in approximately the same position of the end face of the gate electrode and aluminum oxide.

[0016]

That is, as is shown in the schematic figure of TFTs shown in Fig. 1, aluminum oxide 10 is provided on at least the side face of a gate electrode 8, and an electrode 7 for source, drain is connected with a source, drain region 3 approximately in the same position of the end face of this aluminum oxide. With a structure like this, the distance L from said feeding point of said electrode to the channel region can be shortened.

[0017]

To make this distance L perfectly zero is ideal in reducing resistance (in the figure, it is almost zero), but it cannot made in that way because of process technology, for example, some of the source, drain region comes under the gate electrode. However, just to shorten this distance can be very effective.

[0018]

In addition, the aluminum oxide film around the gate electrode is provided on a side face and an upper face, that is, only on exposed portions in Fig. 1. However, in the present invention, it is not necessary for aluminum oxide to be provided on every peripheral portion, except for the portion near the side face to make the distance L short. On the other hand, if aluminum oxide is provided on the whole surface of the gate electrode, this can be utilized as a part of a mask in forming a contact hole because this aluminum oxide is difficult to be etched. Furthermore, because stereoscopic wirings can be easily made on this

aluminum oxide film by crossing wirings of another wiring such as the wiring of the source electrode, it becomes easy to lay out in integration.

[0019]

A structure formed as a result of forming contact holes by self-align method is naturally included in the end portions of the gate electrode and the aluminum oxide approximately made in the same position of the contact hole for the output electrode of source or drain region. The portion formed by difference of the mask which can be aligned by utilizing a photo mask by another method is also included.

[0020]

As a method to form aluminum oxide around this gate electrode, it can be thought of anodic oxidation of this gate electrode for formation. In this anodic oxidation, an aluminum gate electrode is oxidized by electro-chemical reaction while flowing current in an acid solution. However, other method can be also utilized as long as the formed oxide film is minute and has fast oxidation speed.

[0021]

In accordance with Example, this invention will be explained as the following.

[0022]

[Example]

In this example, TFTs of the present invention is utilized for a liquid crystal electro-optic device with a circuit shown in Fig. 4 is shown. In this figure, N channel type thin film transistor 22 and P channel thin film transistor 21 are formed in a complementary structure in each picture element of the liquid crystal device. Each TFT connects the gate electrode to a common signal line 50, and output terminals of the NTFT 22 and the PTFT 21 are connected to the common picture electrode 43. The other output terminals 28 and 35 of each are connected to other signal lines 52 and 53, in an inverter structure. Complementary TFTs can be provided to each picture element by changing the positions of PTFTs and NTFTs, and making a buffer structure.

[0023]

Formation process in forming TFTs of the present invention utilized for a liquid crystal electro-optic device of this structure, and in forming C/TFTs on a glass substrate, is shown in Fig. 3(A) - (F).

[0024]

In Fig. 3(A), a silicon oxide film was formed by 1000 to 3000Å thickness as a blocking layer 24, on an inexpensive glass 1 such

crystallizing glass as AN glass and neo-cera glass, bicor 7913 (made by Corning), or quartz glass which can endure heating of 700℃ or less, such as approximately 600℃.

[0025]

The process condition was oxygen 100% atmosphere, deposition temperature of 150℃, output of 400 - 800W, and pressure of 0.5Pa. As a target material, quartz or single-crystal silicon was utilized, and its deposition speed was 30 - 100Å/minute.

[0026]

A silicon film was formed on this by LPCVD (low pressure gas phase) method, sputter method or plasma CVD method. If it was formed by low pressure gas phase method, deposition was performed by providing disilane (Si_2H_6) or trisilane (Si_3H_8) to a CVD apparatus at 450 - 550℃ which is lower than the crystallizing temperature by 100 - 200℃, such as 530℃. The pressure inside the reaction furnace was made as 30 - 300Pa. The deposition speed was 50 - 250Å/minute. To control the threshold voltage(V_{th}) of NTFTs and PTFTs approximately the same, boron can be added by utilizing diborane during deposition by 1 x 10^{15} - 1 x $10^{18}cm^{-3}$ concentration.

[0027]

If sputtering method is utilized, a background pressure before sputtering was made as 1 x 10^{-5}Pa or less, and single-crystal silicon was utilized as a target, and was performed in an atmosphere of argon added with hydrogen by 20 - 80%, for example, argon was 20%, and hydrogen was 80%. The deposition temperature was 150℃, frequency was 13.56 MHz, and sputtering output was 400 - 800W. Pressure was 0.5Pa.

[0028]

If a silicon film is formed by plasma CVD method, temperature was situated as 300℃ for example, and monosilane (SiH_4) or disilane (Si_2H_6) was utilized. This was introduced in a PCVD apparatus, and deposition was performed by adding high frequency power of 13.56MHz.

[0029]

It is desirable if the film formed by this method has oxygen concentration of 7 x $10^{20}cm^{-3}$ or less. If concentration of this oxygen is high, a semiconductor layer is difficult to be crystallized, so that heat annealing temperature should be made higher or the time of heat annealing should be made longer. If the oxygen concentration is too little, leak current of off condition increases when the semiconductor layer is irradiated by back light utilized for a liquid crystal electro-optic device.

From 4 x 10^{19} to 4 x $10^{21}cm^{-3}$, crystallization can be performed easily by heat annealing of a medium temperature (600℃ or less). On the other hand, the amount of hydrogen in the film was 4 x $10^{20}cm^{-3}$, and was approximately 1 atom% compared with 4 x $10^{22}cm^{-3}$ of silicon.

[0030]

To accelerate crystallization of source, drain region, it is effective to make sensitivity to light weak by making oxygen concentration 7 x $10^{20}cm^{-3}$ or less, desirably 7 x $10^{19}cm^{-3}$ or less, and then by adding oxygen, carbon or nitrogen of 5 x 10^{19} - 5 x $10^{21}cm^{-3}$ in either one of the channel formation regions of the TFTs comprising a pixel by ion injection.

In this way, especially for TFTs making peripheral circuits, contamination of oxygen can be made less, bigger carrier mobility can be obtained, high frequency action can be performed easier, and the TFTs of switching near picture elements can decrease leak current under off condition.

[0031]

In this way, after forming a silicon film of amorphous condition by 500 - 5000Å, for example 1500Å thickness, it was heated at a medium temperature of 450 - 700℃ for 12 - 70 hours in a non-oxide atmosphere. For example, it was kept at 600℃ in a nitrogen or hydrogen atmosphere.

[0032]

Because a silicon oxide film of amorphous structure is formed on the substrate surface under the silicon film, a specific core does not exist by this heating, and the whole portion is equally performed with heat annealing. That is, there is an amorphous structure during deposition, and hydrogen is merely contaminated.

[0033]

The silicon film is changed from amorphous structure to a condition with more regularity by annealing, and a part of it has crystal character. Especially during deposition of silicon, a region with comparatively high regularity especially tries to be crystal by crystallization. However, since silicon atoms present among these regions bond one another, the silicon atoms attract one another. By measuring by laser Raman spectroscopy, a peak shifted to a lower frequency than the peak of single-crystal silicon, $522cm^{-1}$ is observed. Its grain size is seemingly calculated as 50 - 500Å like microcrystal. In fact, there were many regions with high crystal character, and had a cluster structure. A film of semi-amorphous structure with each cluster performed with anchoring could be formed.

[0034]

In such a film as this, for example, when distribution measuring was performed in vertical direction by SIMS (secondary ion mass spectroscopy) method, oxygen was 3.4 x $10^{19}cm^{-3}$, nitrogen was 4 x $10^{17}cm^{-3}$ at a region with minimum amount of additives (impurities) (a surface or a position apart from the surface (inside)). Also, hydrogen was 4 x $10^{20}cm^{-3}$, as 1 atom% when it was compared with silicon as 4 x $10^{22}cm^{-3}$.

[0035]

This crystallization can be performed with 1000Å film thickness and heating at 600℃ (for 48 hours) if oxygen concentration is for example 3.5 x $10^{19}cm^{-3}$. When the concentration is made as 3 x $10^{20}cm^{-3}$, crystallization by annealing at 600℃ can be performed by making the film as thick as 0.3 - 0.5μm. Heating at 650℃ was needed for thickness of 0.1μm for crystallization. That is, the thicker the film became, and the less the concentration of impurities like oxygen became, the easier crystallization became.

[0036]

As a result, the film showed a condition with actually no grain boundary (called as GB). Because carriers can move easily between each cluster through positions performed with anchoring, they have carrier mobility higher than that of poly-crystal silicon with clear GB. That is, hole mobility(uh) = 10 - 200cm^2/Vsec, electron mobility(ue) = 15 -300cm^2 /Vsec.

[0037]

On the other hand, if a film is poly-crystallized by not annealing at a medium temperature as above mentioned but by high temperature annealing at 900 - 1200℃, segregation of impurities in the film happens by solid phase growth from a core. Impurities like oxygen, carbon, and nitrogen increase in GB, and interfere movement of carriers there by making a barrier at GB though mobility in crystal is high. As a result, the fact is mobility of 10cm^2/Vsec or more cannot be obtained easily.

[0038]

In the example of the present invention, because of the reasons above, a silicon semiconductor having semi-amorphous or semi-crystal structure is utilized.

[0039]

In Fig. 3(A), a silicon film is performed with photo etching by the 1st photo mask 1 , a region 21 for PTFTs (channel width of 20μm) is formed in the right side of the figure, and a region 22 for NTFTs is formed in the

left side.

[0040]

A silicon oxide film is formed by 500 - 2000Å thickness, for example, 1000Å, as a gate insulating film 27 on this. This is in the same condition as that of formation of a silicon oxide film as a blocking layer. A little amount of halogen element can be added during deposition to fix sodium ions.

[0041]

After that, an aluminum film is formed on it by 0.3μm thickness. This is patterned by the 2nd photo mask 2. Then a gate electrode 26 for PTFTs and a gate electrode 25 for NTFTs are formed. For example, the channel length is made as 10μm.

[0042]

In Fig. 3(C), a photo resist 31 is formed by photo mask 3, and boron is added to source 28 and drain 30 for PTFTs by dose amount of 1 x $10^{15}cm^{-2}$.

[0043]

As is shown in Fig. 3(D), a photo resist 32 is formed by a photo mask 4. Phosphorus is added to a source 35, drain 33 for NTFTs with dose amount of 1 x $10^{15}cm^{-2}$ by ion injection method.

[0044]

Above mentioned process is performed through a gate insulating film 27. However, in Fig. 3(B), silicon oxide on a silicon film can be removed with gate electrodes 26 and 25 as mask and then boron and phosphorus can be directly performed with ion injection into the silicon film.

[0045]

Nextly, after removing this photo resist 32, heat annealing is performed at 650℃ for 10 - 50 hours again. Then, impurities of source 28, drain 30 of the PTFTs, and source 35, drain 33 region of the NTFTs are activated to become p+ and n+.

[0046]

Channel formation regions 34 and 29 are formed as semi-amorphous semiconductors under the gate electrodes 25 and 26.

[0047]

In this way, even by self-align method, C/TFTs can be formed without heating at 700℃ or more in every process. Therefore, it is not necessary to utilize an expensive substrate like quartz as a substrate material, and is a very appropriate process for a large-area liquid crystal

display device of the present invention.

[0048]

Heat annealing is performed twice in Fig. 3(A) and (D). However, annealing of Fig. 3(A) can be skipped in some cases, and formation time can be shortened by making both of the annealing the heat annealing in Fig. 3(D).

[0049]

Because aluminum is utilized as a gate electrode in the present invention, annealing in Fig. 3(D) process can change hydrogen molecules existing in a gate insulating film by a large amount to hydrogen atoms by an effect of aluminum. Thus the interface state concentration of a gate insulating film can be decreased and disappearance of unnecessary carriers can be decreased at the same time.

[0050]

In Fig. 3(E), aluminum oxide was formed around gate electrodes 25 and 26 by anodic oxidation. Specifically, carbon was utilized as a cathode in 13.7% sulfate solution as a bathing component, being separated from said substrate by about 30cm, and with current concentration of 1 Å/cm ^{2}. In this example, formation was performed with formation rate of about 0.3 μm/minute, and thickness of aluminum oxide is 0.2 - 1 μm, for example, 0.5 μm.

[0051]

In Fig. 3(F), an interlayer insulator 41 was formed as a silicon oxide film by said sputtering method. LPCVD method and photo CVD method can be utilized for formation of this silicon oxide film. For example, it was formed by 0.2 - 1.0 μm thickness. After that, as is shown in Fig. 3 (F), a window 42 for an electrode was formed by photo mask 5. Here, RIE method was utilized, and gate electrodes 25, 26 and aluminum oxide 40 around them were utilized to make the position of the contact hole 42 as close to the channel as possible in self-align way. Thus the distance L between feeding point to the source, drain and the channel region was made to the minimum.

[0052]

Aluminum was formed on the whole portion by sputter method by 0.5 - 1 μm thickness, leads 52, 53 were formed by photo mask 6, and made as electrodes for source regions 28 and 35 of PTFTs and NTFTs as is shown in Fig. 3(G).

[0053]

Organic resin 44 for leveling, such as translucent polyimide resin

was covered on the surface, and opening of holes for electrodes were performed by photo mask 7.

[0054]

As is shown in Fig. 3(F), two TFTs were made in a complemental structure, and ITO (indium-tin oxide film) was formed by sputter method to connect the output terminal to a picture element electrode of a liquid crystal as a transparent electrode. This was etched by photo mask 8, and an electrode 43 was made. This ITO was formed at room temperature to 150℃, and achieved by annealing in oxygen or atmosphere of 200 - 400℃.

[0055]

In this way, PTFT 21, NTFT 22 and an electrode 43 of transparent conductive film were formed on the glass substrate 1.

[0056]

The TFTs was characterized in that the mobility of 20cm^2/Vsec, Vth is -5.9V for PTFTs, and mobility of 40cm^2/Vsec, and Vth of +5.0V for NTFTs.

[0057]

With the use of such semiconductor, a big mobility can be obtained from TFTs which had generally been regarded as impossible. As a result, an active type liquid crystal display device comprising complemental TFTs in each pixel of a liquid crystal electro-optic device could be made for the first time. Peripheral circuits could be also made as ON glass (a method to form them on the same substrate by the same formation process of TFTs).

[0058]

In this example, TFTs of the present invention was used for a liquid crystal electro-optic device. Because frequency character of TFTs is good, moving pictures can be displayed easily. The present invention is applicable to a projection TV, a view finder of a video movie, and a wall TV and the like. As another application, it can be used as a driving element of primary or secondary image sensor, making use of its good frequency character. Its reading speed can fully cope with G4 standard.

[0059]

As above mentioned, a cell for a liquid crystal electro-optic device was formed by a well known method, by utilizing a formed glass substrate and a substrate on which a counter electrode of transparent electrodes in stripes are formed. Liquid crystal material is filled in the cell for this liquid crystal electro-optic device. If TN liquid crystal is

utilized as a liquid crystal material, its space should be approximately 10 μ m, and it is necessary to form an orientation film on both of the transparent conductive films by rubbing.

[0060]

If FLC (ferroelectric) liquid crystal is utilized as a liquid crystal material, operating voltage should be made $\pm$ 20V, space of the cells should be made as 1.5 - 3.5 μ m, for example, 2.3 μ m, and an orientation film should be provided on a counter electrode only, and rubbing treatment should be made.

[0061]

If distributed liquid crystal or polymer liquid crystal was utilized, an orientation film was not needed, and activation voltage was made as $\pm$ 10 - $\pm$ 15V, and the cell space was made as thin as 1 - 10 μ m to make switching speed high.

[0062]

Especially if dispersion liquid crystal was utilized, quantity of light can be made big both as reflection type and transparent type, because a polarizing plate is not needed. Because this liquid crystal has no threshold, big contrast and crosstalk (bad influence on neighboring picture elements) could be removed by making c/TFT type which defines threshold voltage clearly.

[0063]

[Effect of the Invention]

In the present invention, aluminum is utilized as a gate electrode material, and aluminum oxide is provided on the surface of it by anodic oxidation, thus providing a wiring in three dimensional structure having a grade separation. Decrease of frequency character of the device and increase of ON resistance could be prevented by providing a contact hole for source, drain by said gate electrode and aluminum oxide near the electrode to make a feeding point close to the channel.

[0064]

Because aluminum is utilized for a gate electrode, during annealing of the process of forming the element, hydrogen in the gate oxide film can be decreased by changing H_2 to H by catalytic effect of aluminum. Compared with the case of utilizing a silicon gate for interface state (Qss) can be decreased and thus characteristic of an element can be improved.

[0065]

Because source, drain regions of the TFTs were made in self-align, and the position of the contact portion of an electrode for feeding was

decided in self-align way, too, area needed for the TFTs is decreased and thus integration can be improved. If it is utilized as an active element of a liquid crystal electro-optic device, the rate of opening of a liquid crystal panel can be improved.

[0066]

In the present invention, semi-amorphous or semi-crystal was utilized as a semiconductor for such C/TFTs. However, semiconductor of other crystal structure can be utilized for the same purpose, if possible. High speed process was performed by self-align type C/TFTs. However, TFTs can be made not by self-align method without utilizing ion injection method. TFTs of not stagger type but of reverse stagger type or other kinds of TFTs can also be utilized.

[Brief Description of the Invention]

[Fig. 1]

Fig. 1 shows a schematic cross section of an insulating gate type field effect semiconductor device of the present invention.

[Fig. 2]

Fig. 2 shows a schematic cross section of an insulating gate type field effect semiconductor device of the conventional type.

[Fig. 3]

Fig. 3 shows a manufacturing process of an insulating gate type field effect semiconductor device of the present invention.

[Fig. 4]

Fig. 4 shows a circuit figure of a liquid crystal electro-optic device utilizing an insulating gate type field effect semiconductor device of the present invention.

[Explanation of marks]

1.....substrate
2.....semiconductor layer
3.....source, drain region
6.....gate insulating film
7.....source, drain electrode
8.....gate electrode
10.....aluminum oxide

[Name of Document] Abstract

[Abstract]

[Purpose] The present invention offers a structure which makes the distance L between the feeding point to source or drain region neighboring the channel region of TFTs and the end face short.

[Structure] Aluminum is utilized as a gate electrode in the TFTs of the present invention, and at least a side face of said gate electrode is covered with oxide of aluminum. A contact hole for an output electrode of source or drain region is provided approximately in the same position of the end face of the oxide of aluminum in the side face of the gate electrode.

[Selected Figure] Fig. 1